

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

EXCELENCIA SEVERO OCHOA

It's the Memory, Stupid!

Petar Radojkovic

Barcelona Supercomputing Center

31st of October 2026.

Before we start

- The course will be recorded

Today we are touching the memory-performance elephant 🐘 !!!

- It’s Roofline!
- It’s Mess!
- It’s PROFET!
- It’s TopDown!



The best memory-performance tools presented by (one of) the best experts

Tutorial Agenda

Part 1 08:00h – 08:10h

Introduction

Dr. Petar Radojkovic – BSC

Part 2 08:10h – 12:00h

Performance Analysis: Memory Systems & Applications

08:10h – 09:00h · Roofline(s)
Dr. Aleksandar Ilic — INESC-ID, José Brito — INESC-ID

09:00h – 10:00h · Memory System Performance is Messy
Dr. Petar Radojkovic — BSC, Victor Xirau — BSC

10:00h – 10:30h · Coffee Break

10:30h – 11:15h · PROFET: No-stress Performance Prediction
Mariana Carmin — BSC

11:15h – 12:00h · TopDown Microarchitecture Analysis
Anton Hanna — Intel, Victor Xirau — BSC

- **Different views to similar problems**

- In the same day, in the same room, without a bloodshed (we will see about that …)

The second time we are doing this …

memory.bsc.es/news/memory-training-2026

Apps | Bookmarks | BSC | DEEP-SEA | Private | ETP4HPC | SGA2

Memory Systems
for HPC and AI

EVENT February 25, 2026

BSC Training: It's the Memory, Stupid!

More than 100 participants joined our training on memory system profiling and performance analysis.



The course connected 3 European and national initiatives (DARE, BZL & EVITA) and served as a successful chance to gather leading research and industry actors around a shared strategic vision: advancing chip technology, strengthening memory systems, and building open world-class expertise.

With Intel Corporation & INESC-ID. A big thank you to the organizers, speakers, and all participants for the excellent discussions and engagement throughout the session.

Course Materials | BSC LinkedIn Post | DARE Project LinkedIn Post | BZL Article

BSC AI Factory

BSC AI Factory supports AI innovation with access to MareNostrum 5, expert guidance, software, data services, and specialised training for startups, SMEs, public institutions, and researchers.

Universitat Politecnica de Catalunya – BarcelonaTech

The Facultat d'Informàtica de Barcelona (FIB) is one of the top 10 computer science schools in Europe. We have the resources, professors and experience to offer a wide range of courses.

Thank you!

DARE – The Digital Autonomy with RISC-V in Europe

The DARE project aims to boost European digital transformation by developing novel computing and AI technologies

EVITA – The EuroHPC Virtual Training Academy

EVITA is building a high-quality training framework for High-Performance Computing (HPC) and emerging technologies across Europe. EVITA connects leading institutions to deliver recognised qualifications and modular learning content that supports academia, industry, and innovation. Together, we're shaping the future of HPC education.

Barcelona Zettascale Lab

At the Barcelona Zettascala Lab, our mission is to position Europe as a global leader in high-performance computing (HPC). Through innovation in advanced chip design, we aim to strengthen the continent's technological sovereignty and foster a robust ecosystem encompassing both hardware and software.

La Salle Barcelona – Ramon Llull University

International university campus offering studies in ICT Engineering, Architecture, Business, Digital Arts, Animation, Philosophy and Humanities and Health Engineering. Technology, artificial intelligence and innovation to face the challenges of today´s society.

ACAP – High-Performance Computer Architecture

ACAP advances open hardware design and the RISC-V ecosystem to strengthen technological sovereignty over processor IP. The project works on open HPC architectures, domain-specific accelerators, novel memory technologies, and the simulation and modelling methodologies needed to design them.

ST4HPC – Software Tools for HPC

ST4HPC advances the software stack needed to exploit HPC systems built on multi-core processors and accelerators, focusing on programmability, portability and interoperability across parallel, distributed and heterogeneous environments. Its work spans task-based programming models, LLVM compiler extensions for GPU and FPGA acceleration, distributed data management, and edge-to-cloud HPC methodologies.

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It's the Memory, Stupid!

Thank you!



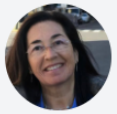
Dr. Aleksandar Ilic
Associate Professor



Dr. Leonel Sousa
Associate Professor



José Brito
PhD Student



Dr. Maria-Ribera Sancho
Head of Education
Education & Training



Dr. Eduard Ayguadé
Department Director
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Dr. Petar Radojkovic
Group Leader
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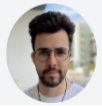

Alexandre Rodrigues
PhD Student



Dr. Harald Servat
Software Enabling and Optimization Engineer



Dr. Xavier Martorell
Group Leader
Parallel Programming Models



Dr. Toni Peña
Group Leader
Accelerators and Communications for HPC



Victor Xirau
Research Engineer
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Javier Beiro
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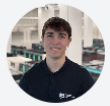
COMPUTER ARCHITECTURE FOR PARALLEL PARADIGMS GROUP MANAGER
Computer Sciences - Computer Architecture for Parallel Paradigms



Claudia Romo
CPU Performance Architect



Anton Hanna
CPU Core Architect



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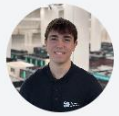

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